

# **GPS16160/GPS6160**

## **User's Manual**

***GPS PC/104 Module***



RTD Embedded Technologies, Inc.

*"Accessing the Analog World"®*

ISO9001 and AS9100 Certified

BDM-610020037  
Rev. C

# **GPS16160/GPS6160**

## **User's Manual**



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## Manual Revision History

### Rev A Manual converted to RTD format.

- New manual revision system, based on ISO9001:2000.
- Board photo updated to show the new RTD USA design (rev AA).
- Significant re-work of content, based on GPS140 manual (BDM-610020004).
- Updated information to reflect the new iTrax03-02 GPS engine.
- Added note about previous versions which used iTrax02 engine.
- Added information about Windows serial mouse detection issues.

### Rev B Changed to support GPS16160

- Added 1 PPS interrupt capability
- Added utility connector with 1 PPS, and user interface signals
- Added bit-programmable digital I/O
- Added RTD ISA ID
- Added 1 PPS to UART CD
- Software backwards compatible to GPS6160

### Rev C Update for AS9100 Certification

- Updated cover page to mention ISO9000 and AS9100 Certification
- Added WAAS support in list of board features
- Corrected ITRAX update rate from 5Hz to 3Hz
- Corrected Fastrax web link

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# Introduction

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## ***Product Overview***

The GPS16160 is designed to provide global positioning system (GPS) for PC/104 based systems. Included on the GPS16160 is a Fastrax iTrax03-02 GPS Receiver module.

The GPS16160 has a UART chip that permits communication with either serial port on the GPS receiver module over the PC/104 bus without using other serial ports in the PC/104 system. The GPS supports iTalk binary protocol and National Marine Electronics Association (NMEA-0183) messages.

## ***Board Features***

### **GPS16160 Features**

- Direct connection to the Fastrax iTrax03-02 GPS receiver module selectable between the iTrax binary port or the NMEA port
- GPS message formats
  - iTalk Binary
  - NMEA
- Serial communication interrupt
- 1 PPS on UART carrier detect
- 1 PPS interrupt
- GPS6160 backwards compatible
  - Board can be factory configured to be exactly like a GPS6160, contact factory for more information
- PC/104 compliant
- Support Wide Area Augmentation System (WAAS)

### **GPS Receiver**

Integrated on your GPS16160 is a fast fix 12-channel low power iTrax03-02 GPS receiver from Fastrax. This GPS receiver will work reliably in a variety of installations. The receiver will work with either 3.3V or 5.0 Volt active or with passive antennas. The power consumption of the GPS receiver is 125 mW fully operational. The iTrax03-02 features a fast 1 to 3 Hz update rate. Two output formats are available: the NMEA-0183 ASCII protocol or the iTalk proprietary binary protocol. Each protocol has its own dedicated serial interface.

## ***I/O Interfaces***

The GPS16160 can be controlled and monitored by software through the dedicated serial port of the module.

### **16C550 Compatible UART**

The GPS receiver module communicates through a dedicated UART channel allowing other serial ports in the system to be free for the user.

### **Connector Description**

The GPS antenna interface is a female MMCX type miniature coaxial connectors. Connect your antenna directly to the GPS16160 antenna connector, or use a short cable inside your enclosure to connect to a

feed through connector to allow connection of the antenna to the wall of your enclosure. The GPS module supplies up to 100 mA of 3.3 or 5.0 VDC for antenna LNA.

All other I/O connections to the GPS16160 use 0.1" header type terminals.

## ***Available Options***

The GPS16160 is available as a starter kit, bundled with an active antenna. It may also be purchased as an IDAN module for integration into an RTD IDAN system.

The following is a summary of the different GPS16160 configurations:

<b>Part Number</b>	<b>Description</b>
GPS16160	GPS16160 GPS with Fastrax iTrax03-02 module
SK-GPS16160	GPS16160 with active antenna for GPS
IDAN-GPS16160S	GPS16160 mounted in an IDAN frame
IDAN-SK-GPS16160S	GPS16160 mounted in an IDAN frame with active antenna for GPS

For antenna specifications, please refer to the "Additional Information" chapter of this manual.

## ***Getting Technical Support***

If you are having problems with your system, please try the following troubleshooting steps:

- **Simplify the System** – Remove modules one at a time from your system to see if there is a specific module that is causing a problem.
- **Swap Components** – Try replacing parts in the system one-at-a-time with similar parts to determine if a part is faulty or if a type of part is configured incorrectly.

If problems persist, or you have questions about configuring this product, obtain the PCI BIOS listing information of the GPS16160 and other modules in the system. After you have this information, contact RTD Embedded Technologies via the following methods:

Phone: +1-814-234-8087

E-Mail: [techsupport@rtd.com](mailto:techsupport@rtd.com)

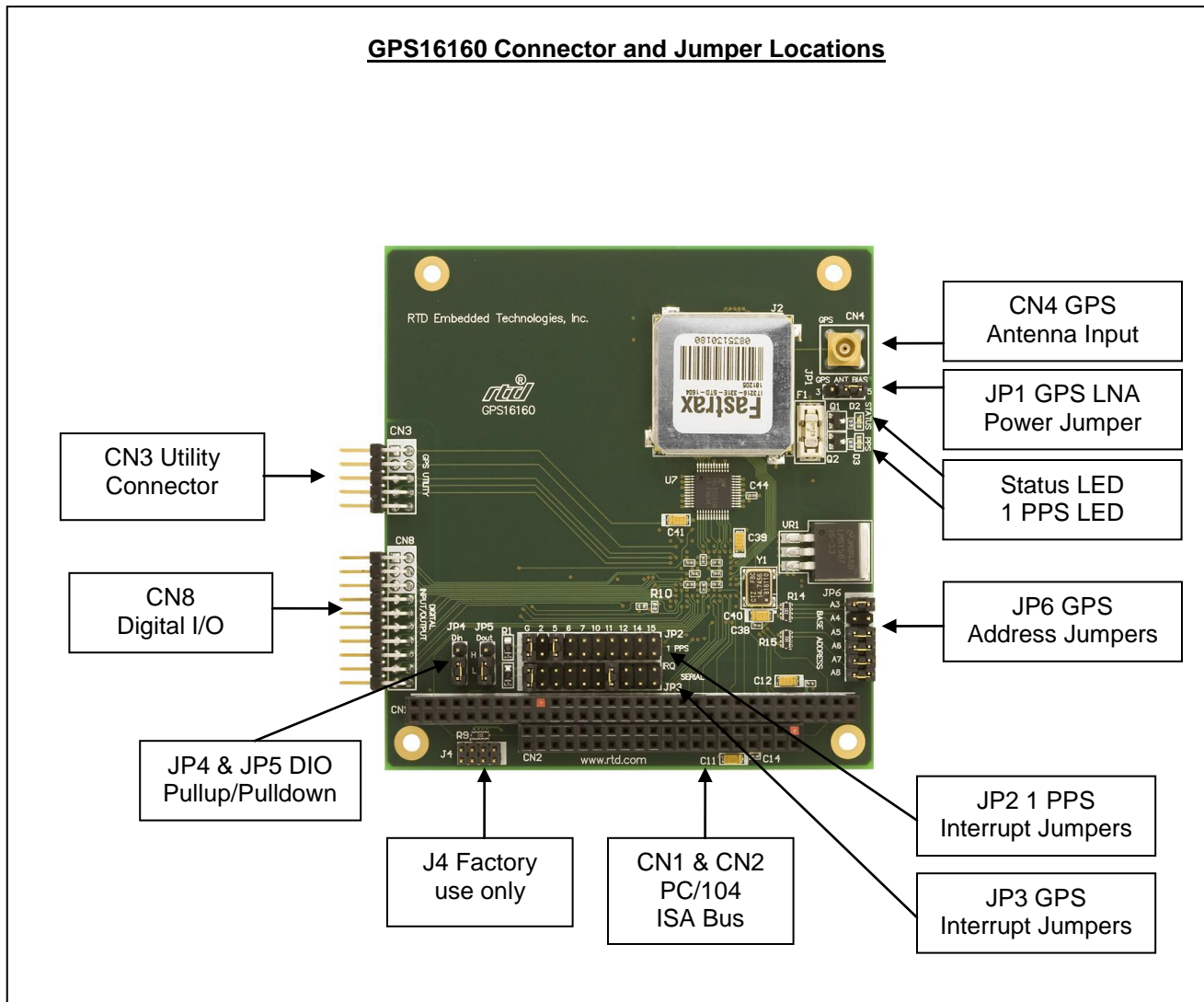
Be sure to check the RTD web site (<http://www.rtd.com>) frequently for product updates, including newer versions of the board manual and application software.



# Board Connections

## Connector and Jumper Locations

The following diagram shows the location of all connectors and jumpers on the GPS16160. Future revisions of the GPS16160 may have cosmetic differences. For a description of each jumper and connector, refer to the following sections.

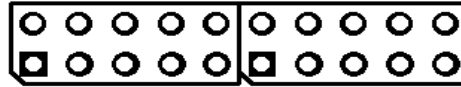


## External I/O Connections

The following sections describe the external I/O connections of the GPS16160.

## CN8 – Digital Input/Output Connector

The GPS16160 offers 16 bit-programmable digital I/O lines. These can be pulled high or low through 10K Ohm resistors using JP4 to control bits 0 – 7 and JP5 to control bits 8 - 15.

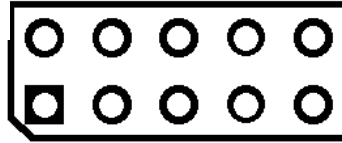


Pin	Name	CN8 Description GPS16160 Mode	CN8 Description GPS6160 Mode
1	GND	Ground	Ground
2	DIO0	Digital Input/Output Bit 0 or 1PPS	Digital Output Bit 0
3	DIO1	Digital Input/Output Bit 1	Digital Output Bit 1
4	DIO2	Digital Input/Output Bit 2	Digital Output Bit 2
5	DIO3	Digital Input/Output Bit 3	Digital Output Bit 3
6	DIO4	Digital Input/Output Bit 4	Digital Output Bit 4
7	DIO5	Digital Input/Output Bit 5	Digital Output Bit 5
8	DIO6	Digital Input/Output Bit 6	Digital Output Bit 6
9	DIO7	Digital Input/Output Bit 7	Digital Output Bit 7
10	+5 VDC	+5 Volts DC	+5 Volts DC
11	GND	Ground	Ground
12	DIO8	Digital Input/Output Bit 8	Digital Input Bit 0
13	DIO9	Digital Input/Output Bit 9	Digital Input Bit 1
14	DIO10	Digital Input/Output Bit 10	Digital Input Bit 2
15	DIO11	Digital Input/Output Bit 11	Digital Input Bit 3
16	DIO12	Digital Input/Output Bit 12	Digital Input Bit 4
17	DIO13	Digital Input/Output Bit 13	Digital Input Bit 5
18	DIO14	Digital Input/Output Bit 14	Digital Input Bit 6
19	DIO15	Digital Input/Output Bit 15	Digital Input Bit 7
20	+5 VDC	+5 Volts DC	+5 Volts DC

Pin	Name	CN8 Power On Defaults
1	GND	Ground
2	DIO0	Digital Output Bit 0
3	DIO1	Digital Output Bit 1
4	DIO2	Digital Output Bit 2
5	DIO3	Digital Output Bit 3
6	DIO4	Digital Output Bit 4
7	DIO5	Digital Output Bit 5
8	DIO6	Digital Output Bit 6
9	DIO7	Digital Output Bit 7
10	+5 VDC	+5 Volts DC
11	GND	Ground
12	DIO8	Digital Input Bit 0
13	DIO9	Digital Input Bit 1
14	DIO10	Digital Input Bit 2
15	DIO11	Digital Input Bit 3
16	DIO12	Digital Input Bit 4
17	DIO13	Digital Input Bit 5
18	DIO14	Digital Input Bit 6
19	DIO15	Digital Input Bit 7
20	+5 VDC	+5 Volts DC

## CN3 – GPS Utility Connector

The GPS16160 provides 1 PPS delayed through the EPLD (7.5ns max). Also, user interface bits of the GPS are available. The pin out of the external connector CN3 is shown below.



Pin	Direction	Name	CN3 Description
1	Power	+5V	Power
2	Reserved	R	Reserved
3	Ground	GND	Ground
4	Output	1PPS	1 PPS from GPS
5	Ground	GND	Ground
6	Output	UI-A	GPS Mode
7	Output	UI-B	GPS Fix Status
8	Output	UI-C	GPS Valid Fix
9	Ground	GND	Ground
10	Ground	GND	Ground

The UI Indicators are updated synchronously at 1 Hz rate. The high state duty cycle is either 0% (Continuously low state), 20% (Short blink), 80% (Long blink) or 100% (Continuously high state).

UI Bit	High Ratio	Description
A	Continuously low state	Power Off or Sleep mode
	Short blink 20	Normal mode, Navigation stopped
	Long blink 80	Normal mode, Navigation started
B	Continuously low state	Navigation stopped or not tracking satellites
	Short blink 20	Tracking satellites but not enough information to calculate pseudo-ranges
	Long blink 80	Pseudorange information available but not navigating
	Continuously high state	Navigating, valid fix
C	Low state	Valid fix available
	High state	No valid fix

## Jumpers

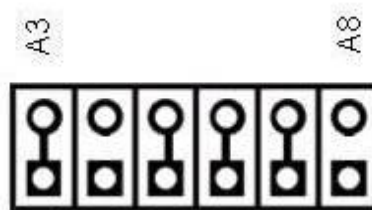
The following sections describe the jumper configuration options available on the GPS16160. For a reference that shows the location of each set of jumpers, refer to the diagram of the GPS16160 at the beginning of this chapter. The default factory jumper settings are listed in the following table:

Jumper	Description	Default Factory Setting
JP1	GPS Active Antenna Power (100 ma max)	1-2 - +5.0 VDC (default) 2-3 - +3.3 VDC Open for passive antennas
JP2	1 PPS Interrupt Jumper	Default No Interrupt and G
JP3	GPS Interrupt Jumper	Default Interrupt 5 and G
JP4	Pull-up or Pull-down for DIO0-7	1-2 - Pull-up 2-3 - Pull-down (default) No connect - Neither
JP5	Pull-up or Pull-down for DIO8-15	1-2 - Pull-up 2-3 - Pull-down (default) No connect - Neither
JP6	GPS Base Address Jumper (A8 - A3, A9 is always high)	Default 2E8h

### GPS (JP6) Base Address Jumpers (Default: = 2E8h)

The base address selection jumpers (A3 through A8) allow you to set the base address of the first UART that connects to the GPS module. Any software that accesses the board will do so through reads and writes to the I/O address set by the jumpers. To function properly, the I/O address the software is expecting must match the base address set by the jumpers.

As shown in the figure below, A3 is located at the left end of the jumper block, while A8 is located at the right end:



The table on the following pages shows the possible base address settings for the GPS16160. All base addresses are in hexadecimal. An 'X' indicates a closed jumper, while an empty cell indicates an open jumper.

Base Address (Hexadecimal)	Jumpers					
	A8	A7	A6	A5	A4	A3
200						
208						X
210					X	
218					X	X

Base Address (Hexadecimal)	Jumpers					
	A8	A7	A6	A5	A4	A3
220				X		
228				X		X
230				X	X	
238				X	X	X
240			X			
248			X			X
250			X		X	
258			X		X	X
260			X	X		
268			X	X		X
270			X	X	X	
278			X	X	X	X
280		X				
288		X				X
290		X			X	
298		X			X	X
2A0		X		X		
2A8		X		X		X
2B0		X		X	X	
2B8		X		X	X	X
2C0		X	X			
2C8		X	X			X
2D0		X	X		X	
2D8		X	X		X	X
2E0		X	X	X		
<b>2E8</b>		<b>X</b>	<b>X</b>	<b>X</b>		<b>X</b>
2F0		X	X	X	X	
2F8		X	X	X	X	X
300	X					
308	X					X
310	X				X	
318	X				X	X
320	X			X		
328	X			X		X
330	X			X	X	
338	X			X	X	X
340	X		X			
348	X		X			X
350	X		X		X	
358	X		X		X	X
360	X		X	X		
368	X		X	X		X
370	X		X	X	X	
378	X		X	X	X	X
380	X	X				
388	X	X				X
390	X	X			X	
398	X	X			X	X
3A0	X	X		X		
3A8	X	X		X		X
3B0	X	X		X	X	
3B8	X	X		X	X	X

Base Address (Hexadecimal)	Jumpers					
	A8	A7	A6	A5	A4	A3
3C0	X	X	X			
3C8	X	X	X			X
3D0	X	X	X		X	
3D8	X	X	X		X	X
3E0	X	X	X	X		
<b>3E8</b>	<b>X</b>	<b>X</b>	<b>X</b>	<b>X</b>		<b>X</b>
3F0	X	X	X	X	X	
3F8	X	X	X	X	X	X

By default, the GPS16160 comes configured with a base address of 0x2E8 for the GPS UART.

When selecting a base address for the GPS16160, please observe the following guidelines:

- Every device in your PC/104 system must have a unique base address! When selecting a base address for the GPS16160, make certain that it does not conflict with any other devices.
- Base addresses 0x3F8 and 0x2F8 are typically used by serial ports COM1 and COM2, respectively. If you wish to use one of those base addresses, you will need to disable any conflicting serial port.
- Some operating systems expect UART devices to be located at the standard serial port base addresses (0x3F8, 0x2F8, 0x3E8, and 0x2E8). Setting your GPS16160 to one of these addresses can make system setup and configuration easier.

## IRQ Jumpers for GPS (JP3) (Default: IRQ 5 and G Jumper closed)

The IRQ selection jumpers allow you to set the IRQ used by the serial port UART of the GPS16160. The GPS16160 can be configured for any one of the following IRQs: 2, 5, 6, 7, 10, 11, 12, 14, or 15. The IRQ can be set by closing the appropriately labeled jumper on the board.

The UART's carrier detect signal, which is driven by the GPS 1 PPS, can be an interrupt source.

---

**Note:** Typically IRQs cannot be shared; although there are some special cases (see "The G Jumper" later in this document). In general, the IRQ you select should not be used by any other devices in your system.

---

## IRQ Jumper for 1 PPS (JP2) (Default: G Jumper closed)

The IRQ selection jumpers allow you to set the IRQ used by the 1 PPS signal from the GPS of the GPS16160. The GPS16160 can be configured for any one of the following IRQs: 2, 5, 6, 7, 10, 11, 12, 14, or 15. The IRQ can be set by closing the appropriately labeled jumper on the board.

## Reserved IRQs

Some of the IRQ choices on the GPS16160 may already be used by your CPU's onboard peripherals. Some commonly-used IRQs are:

- IRQ 2/9 is used by some VGA controllers.

- IRQ 5 or 7 may be used by the CPU's parallel port. Check your CPU's configuration to avoid a conflict.
- IRQ 12 is used by the PS/2 mouse. To use this IRQ, you will need to remove the PS/2 mouse from the system. Some CPUs also require a BIOS setting to disable the PS/2 mouse controller.
- IRQ 14 is used by the primary IDE controller. To use this IRQ, you will need to disable the primary IDE controller.
- IRQ 15 is used by the secondary IDE controller. To use this IRQ, you will need to disable the secondary IDE controller.

## The G Jumper

The GPS16160 supports shared interrupts as defined by the PC/104 specification. This sharing is accomplished via the G jumper, which is located adjacent to the IRQ jumpers. The G jumper installs a 1K-ohm resistor to pull the signal to the low state, allowing an interrupt to drive the signal high. To share interrupts, configure the devices for the same IRQ, then close the G jumper on one (and only one) of the devices.

When using interrupt sharing, consider the following guidelines:

- An interrupt can only be shared if all devices on the IRQ support it. If you have two sharing and one non-sharing device on the same IRQ, it will not work.
- To share interrupts, the system's drivers and operating system must support it. The Interrupt Service routines must be written to check all devices on an IRQ when the interrupt is detected. Many popular operating systems do not support interrupt sharing for ISA devices.

---

**Note:** If you are not sharing interrupts, make sure you leave the GPS16160's G jumper closed!

---

## LED Indicators

D2 (Status) –

GPS16160 mode

- Continuously low state – Navigation stopped or not tracking satellites
- Short blink 200 milliseconds on and 800 milliseconds off – Tracking satellites but not enough information to calculate pseudo-ranges
- Long blink 800 milliseconds on and 200 milliseconds – Pseudo range information available but not navigating
- Continuously high state – Navigating, Valid fix

GPS6160 Mode

- Off = NMEA protocol, On = iTalk protocol

D3 (PPS) – GPS 1 Pulse Per Second (1 PPS)

# Board Installation

---

## *Installing the Hardware*

The GPS16160 can be installed into a PC/104. It can be located almost anywhere in the stack, above or below the CPU as long as all PC/104 bus constraints are met.

## **Static Precautions**

Keep your board in its antistatic bag until you are ready to install it into your system! When removing it from the bag, hold the board at the edges, and do not touch the components or connectors. Handle the board in an antistatic environment, and use a grounded workbench for testing and handling of your hardware.

## **Steps for Installing**

1. Shut down the PC/104 system and unplug the power cord.
2. Ground yourself with an anti-static strap.
3. Line up the pins of the GPS16160's PC/104 connector with the PC/104 bus of the stack and gently press the board onto the stack. The board should slide into the matching PC/104 connector easily. Do not attempt to force the board, as this can lead to bent/broken pins.
4. Attach the external antennas to the MMCX connectors.
5. If any boards are to be stacked above the GPS16160, install them.
6. Attach any necessary cables to the PC/104 stack.
7. Re-connect the power cord and apply power to the stack.
8. Apply power to the system, and verify that all of the hardware is working properly. Once power is applied, the GSM module and GPS receiver will automatically initialize.

## *Configuring Software*

After physically installing the GPS16160, your operating system must be configured to recognize the new board.

## **Serial Port Setup**

The GPS16160 uses a standard serial port UART for host communication. Therefore, you must "install" the serial port under your host operating system for the GPS16160 to be recognized.

If the GPS16160 was installed using standard serial port base addresses (0x3F8, 0x2F8, 0x3E8, or 0x2E8), your operating system may detect the UART channel automatically. If they are not auto-detected, or were configured with a non-standard base address, the serial port will need to be configured manually.

The procedure for installing and configuring the serial ports will vary depending on the operating system. Consult the operating system's documentation for instructions on how to do this.



---

**Note:** Under Windows 2000/XP, the GPS may be incorrectly detected as a Serial Mouse, causing erratic mouse cursor behavior. This issue has been documented by Microsoft, and can be resolved by a Registry change. For more information, refer to Microsoft Knowledge Base Article 283063.

---

## Installing Drivers

The GSM and GPS are accessed via the serial port UART, and therefore need no special drivers. However, the digital I/O and certain control functions are accessed via their own registers (located at Base Address + 0x400).

To use the digital I/O, or to use these control functions (e.g. switch GPS protocols from NMEA to iTalk), you will need to access these registers. This is typically done through a “driver”. RTD provides drivers for supported operating systems. If you are using an operating system not supported by RTD, you will need to develop your own driver. You may also be able to access the registers directly.

---

**Note:** If you are only using ASCII/NMEA GPS functions, without digital I/O or the iTalk protocol, there is no need to install any special drivers.

---

# Hardware Description

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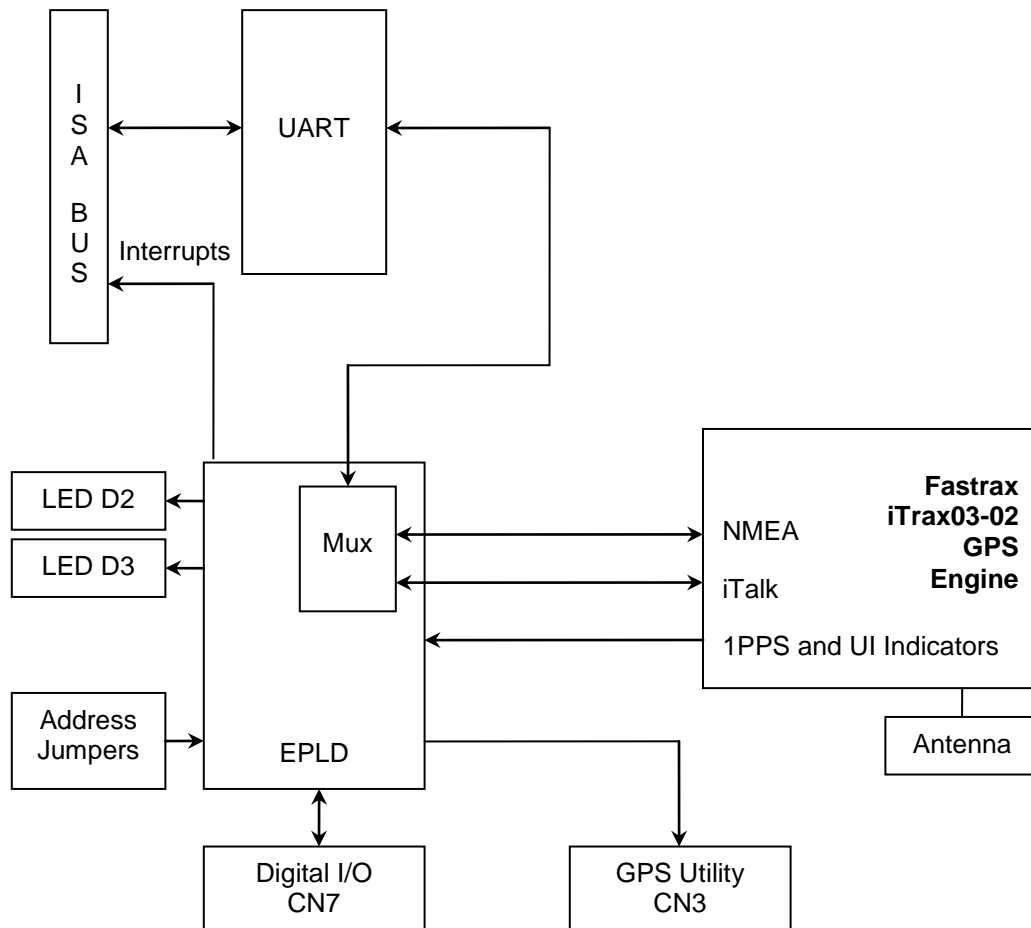
## Overview

This chapter describes the major hardware building blocks of the GPS16160. The components discussed in this chapter include:

- Fastrax iTrax03-02 GPS Receiver Module
- Antenna

## Block Diagram

Below is a block diagram of the GPS16160.



## ***Fastrax iTrax03-02 GPS Receiver***

Integrated on the GPS16160 is an iTrax03-02 low power fast-fix 12-channel GPS receiver from Fastrax. This GPS receiver is especially designed for portable and mobile applications. This version of the GPS does not support differential operation.

The iTrax03-02 sensitivity provides continuous tracking and navigation down to a signal level of –152 dBm and a cold start TTFF of 40 seconds (no initialization), 33 seconds for warm start (almanac) and four seconds for quick start. Even with this performance, the power consumption is approximately 125mW with a 1s update-rate. This figure does not include the active antenna power consumption. A complete GPS configuration program for the iTrax03-02 GPS Workbench is available from the manufacturer's website at [www.fastrax.com](http://www.fastrax.com). This program allows you to completely reconfigure the operation of the GPS receiver.

GPS data is output only when the receiver has a fix. The GPS16160 is configured to output NMEA-0183 version 3.0 data by default and selectable Fastrax's binary protocol iTalk.

### **GPS module interfaces**

The iTrax03-02 GPS is connected to the host computer through a dedicated ISA serial port. Carrier Detect of the serial port is driven by the 1 PSS signal. The default configuration for the serial ports is:

#### **NMEA Interface (Default)**

- 4800 baud
- 8 data bits
- No parity
- 1 stop bit
- No flow control

#### **iTalk Interface (selectable in I/O register)**

- 115,200 baud
- 8 data bits
- No parity
- 1 stop bit
- No flow control

#### **1 PPS on Carrier Detect**

- Carrier detect input (bit 7 of MSR) = '1' when 1 PPS is high
- Carrier detect input = '0' when 1 PPS is low
- Carrier detect delta (bit 3 of MSR) goes high every time 1 PPS changes state. It is cleared to 0 when the MSR is read.

### **GPS Antenna considerations**

Most GPS antennas are "active" which means they have a low noise amplifier (LNA) built into the antenna that requires a power source for the GPS module. While the GPS16160 will work with a passive antenna, better performance will be achieved with an active antenna. The GPS16160 provides either +5.0 V or +3.3 V for active GPS antennas. A three-terminal header is used to select the operating voltage of the antenna. The internal gain of the GPS receiver can be

adjusted to low-output signals or even to interface to passive antennas. This operation is normally not needed, but it can be done using the Fastrax GPS Workbench program.

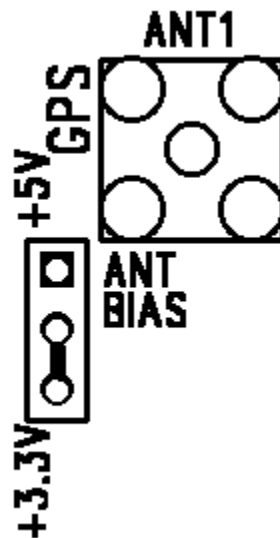


Fig. 4-2 GPS antenna bias voltage

A 90 degree 50 Ohm OSX connector should be selected to directly plug into the antenna connector on the board. High quality low loss antenna cable should be used. Try to reduce the number of connectors on the cable to minimize signal reflections. Signal reflections on the antenna line may cause incorrect readings for altitude information.

## ***GPS16160 Digital I/O***

The GPS16160 has 16 bit-programmable digital I/O bits. RTD's driver software exports functions to use the digital I/O and the operation is covered in the Drivers Users Manual. JP4 controls a 10K Ohm pull up/down on DIO bits 1-8 and JP5 controls a 10K Ohm pull up/down on DIO bits 9 - 16. For programming information see GPS16160 Module Programming section.

## ***Interrupts***

Interrupts are used to notify the host CPU that an event happened on a particular device. In general, interrupts are more efficient than a polling technique, where the CPU must query the device status at regular intervals. Devices that use interrupts have a special connection to the CPU, called an *interrupt request line* (IRQ). When the device needs the CPU's attention, it asserts the IRQ line. Once the interrupt has been processed, the IRQ line is de-asserted.

The GPS16160 uses one ISA interrupt for the GPS UART and another for the 1 PPS. However, it will not actually generate interrupts unless the Interrupt Enable register has been properly programmed.

Since the GPS16160 has 16C550 UARTs, it supports all of the standard serial port interrupt events. These events include:

- Received data available

- Transmit buffer empty
- Line Status Register change
- Modem Status Register change

A detailed explanation of serial port interrupts is beyond the scope of this manual. For more information, consult a serial port programming reference. The chapter titled “Additional Information” lists some resources to help the user.

---

**Note:** When the UART clock is running at a higher frequency, transmit/receive interrupts will happen more frequently. Many operating systems cannot process interrupts quickly enough to handle this load. When developing your software, be sure to consider the operating system’s limitations.

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# GPS16160 Module Programming

This chapter shows you how to program and use your GPS16160. It provides a general description of the I/O map.

## Defining the I/O Map

The I/O map of the GPS16160 occupies a group of eight bytes of host PC I/O space. This window is freely selectable by the user by jumpers JP6. After setting the base address (GPS Base) you have access to the internal resources of the GPS16160 control logic. The board also has 16 digital I/O lines that can be accessed several ways.

ADDR (hex)	REGISTER	DIR	COMMENTS
GPS BASE + 0	TXD	O	Standard 16C550 UART Registers
	RXD	I	
	BAUD div. Low	I/O	
GPS BASE + 1	BAUD div. High	I/O	
	IRQ enable	I/O	
GPS BASE + 2	IRQ ID	I/O	
GPS BASE + 3	Line control	I/O	
GPS BASE + 4	Modem control	I/O	
GPS BASE + 5	Line status	I/O	
GPS BASE + 6	Modem status	I/O	
GPS BASE + 400h	Digital I/O	I/O	GPS6160 compatibility DIO
GPS BASE + 401h	GPS status	I/O	Configuration registers
GPS BASE + 402h	Reserved		Reserved
GPS BASE + 403h	Reserved		Reserved
The following registers are not in the GPS6160 version			
GPS BASE + 404h	Digital I/O	I/O	Digital I/O bits 0 - 7
GPS BASE + 405h	Digital I/O	I/O	Digital I/O bits 8 – 15
GPS BASE + 406h	Digital I/O Dir	I/O	Digital I/O direction bits 0 - 7
GPS BASE + 407h	Digital I/O Dir	I/O	Digital I/O direction bits 8 - 15
GPS BASE + 800h	RTD ID Data	Read	Read next RTD ID Character

GPS BASE + 801h	RTD ID Data	Read	Read next RTD ID Character
GPS BASE + 802h	Reset RTD ID	Read	Reset RTD ID counter

## UART Interfaces

The primary method of interfacing with the GPS16160 is via the UART. Once the GPS16160 is properly installed and configured in the system, the board will appear as an extra COM port to the CPU. The COM port is attached to the GPS module.

### GPS I/O UART (GPS BASE + 0 to GPS BASE + 7)

These are the UART registers for the GPS module. These resources are not described in detail, since they are mapped as a standard PC serial port. For more details on the EXAR 16C550 UART chip programming please download the component specific data from the website: <http://www.exar.com>. Detailed serial port programming tips are not within the scope of this manual. However books and web sites explaining serial port programming are readily available.

### GPS Status – R/W at GPS BASE + 401h (00h after reset)

GPS Status – Write GPS BASE + 401h		
Bit 0	CH_SEL	0 – NMEA mode; 1 – iTalk protocol
Bit 1	GPS_RESET	1 – Reset GPS receiver, 0 – GPS active
Bit 2	RESERVED	
Bit 3	/EN_INT	0 – GPS interrupt enabled; 1 – disabled
Bit 4	RESERVED	
Bit 5	RESERVED	
Bit 6 GPS16160 only	1PPS/DIO0	0 = DIO0, 1 = 1PPS, (default = 0)
Bit 7	RESERVED	

GPS Status – Read GPS BASE + 401h		
Bit 0	CH_SEL	0 – NMEA mode; 1 – iTalk protocol
Bit 1	GPS_RESET	1 – Reset GPS receiver, 0 – GPS active
Bit 2 GPS16160 only	Continuously low	Navigation stopped or not tracking satellites
	Short blink 20%	Tracking satellites but not enough information to calculate pseudo-ranges
	Long blink 80%	Pseudo-range information available but not navigating
	Continuously high	Navigating, Valid fix
Bit 3	/EN_INT	0 – GPS interrupt enabled; 1 – disabled
Bit 4	RESERVED	
Bit 5	RESERVED	
Bit 6 GPS16160 only	1PPS/DIO0	0 = DIO0, 1 = 1PPS
Bit 7 GPS16160 only	1PPS	1 Pulse Per Second from GPS

## Digital I/O

GPS16160 allows bit programmable direction for all digital I/O bits. GPS6160 compatibility is described later. Note the digital I/O registers are accessed at 404h – 407h above the GPS COM port.

Digital I/O Map			
ADDR (hex)	REGISTER	DIR	COMMENTS
GPS BASE + 404h	Digital I/O	I/O	Digital I/O bits 0 - 7
GPS BASE + 405h	Digital I/O	I/O	Digital I/O bits 8 – 15
GPS BASE + 406h	Digital I/O Dir	I/O	Digital I/O direction bits 0 - 7
GSM BASE + 407h	Digital I/O Dir	I/O	Digital I/O direction bits 8 - 15

### Advanced Digital I/O – R/W at GSM BASE + 404h

These addresses are used to interface to the digital I/O port. The 16 bits each have a direction bit. If the direction bit is set to output, a value written to the data bit is provided on the connector. A read will result in the value on the connector pin (i.e. the output value). If the direction is set to input, a value written to the data bit is ignored and a read will result in the value on the connector pin.

Digital I/O Data – Write/Read GPS BASE + 404h (Reset = 00h)		
Bit 0	I/O 0	CN8 Pin 2
Bit 1	I/O 1	CN8 Pin 3
Bit 2	I/O 2	CN8 Pin 4
Bit 3	I/O 3	CN8 Pin 5
Bit 4	I/O 4	CN8 Pin 6
Bit 5	I/O 5	CN8 Pin 7
Bit 6	I/O 6	CN8 Pin 8
Bit 7	I/O 7	CN8 Pin 9

Digital I/O Data – Write/Read GPS BASE + 405h (Reset = 00h)		
Bit 0	I/O 8	CN8 Pin 12
Bit 1	I/O 9	CN8 Pin 13
Bit 2	I/O 10	CN8 Pin 14
Bit 3	I/O 11	CN8 Pin 15
Bit 4	I/O 12	CN8 Pin 16
Bit 5	I/O 13	CN8 Pin 17
Bit 6	I/O 14	CN8 Pin 18
Bit 7	I/O 15	CN8 Pin 19

Digital I/O Direction – Write/Read GPS BASE + 406h (Reset = FFh)		
Bit 0	I/O 0	0 = CN8 Pin 2 is an input, 1 = output



Digital I/O Direction – Write/Read GPS BASE + 406h (Reset = FFh)		
Bit 1	I/O 1	0 = CN8 Pin 3 is an input, 1 = output
Bit 2	I/O 2	0 = CN8 Pin 4 is an input, 1 = output
Bit 3	I/O 3	0 = CN8 Pin 5 is an input, 1 = output
Bit 4	I/O 4	0 = CN8 Pin 6 is an input, 1 = output
Bit 5	I/O 5	0 = CN8 Pin 7 is an input, 1 = output
Bit 6	I/O 6	0 = CN8 Pin 8 is an input, 1 = output
Bit 7	I/O 7	0 = CN8 Pin 9 is an input, 1 = output

Digital I/O Direction – Write/Read GPS BASE + 407h (Reset = 00h)		
Bit 0	I/O 8	0 = CN8 Pin 12 is an input, 1 = output
Bit 1	I/O 9	0 = CN8 Pin 13 is an input, 1 = output
Bit 2	I/O 10	0 = CN8 Pin 14 is an input, 1 = output
Bit 3	I/O 11	0 = CN8 Pin 15 is an input, 1 = output
Bit 4	I/O 12	0 = CN8 Pin 16 is an input, 1 = output
Bit 5	I/O 13	0 = CN8 Pin 17 is an input, 1 = output
Bit 6	I/O 14	0 = CN8 Pin 18 is an input, 1 = output
Bit 7	I/O 15	0 = CN8 Pin 19 is an input, 1 = output

## RTD ISA ID

ADDR (hex)	REGISTER	DIR	COMMENTS
BASE + 800h	RTD ID Data	Read	Read next RTD ID Character
BASE + 801h	RTD ID Data	Read	Read next RTD ID Character
BASE + 802h	Reset RTD ID	Read	Reset RTD ID counter

I/O map of the GPS16160 RTD ISA ID

## BA + 800h/BA + 801h RTD ID Data (read only, 8-bit or 16-bit)

RTD ID is a method to identify a board on the ISA bus. There are two 8-bit registers mapped at **BA + 800h** and **BA + 801h**. This can be either the GSM base address or the GPS base address. The registers can be read as two 8-bit or one 16-bit. An internal pointer is auto-incremented with every read to either address so the data read will step through each index as indicated below. The pointer is set to zero at reset and can be reset to zero by a read to **BA + 802h**.

## BA + 802h RTD ID Reset Pointer (read only, 8-bit only)

A read to **BA + 802h** will set the internal pointer to zero. The pointer is set to zero at reset.

## RTD ID Data Read Indexes

Index	Data	8-Bit Read	16-Bit Read
0	Device ID	60h	6160h
1	Device ID	61h	—
2	RTD Vendor ID	35h	1435h

3	RTD Vendor ID	14h	—
4	EPLD Revision	Revision LSD	Revision
5	EPLD Revision	Revision MSD	—
6–9	Reserved	Ignore	Ignore
10	Board Name String	G	GP
11	Board Name String	P	—
12	Board Name String	S	S1
13	Board Name String	1	—
14	Board Name String	6	61
15	Board Name String	1	—
16		6	60
17		0	—
18	Board Name String	<nul>	<nul><nul>
19	Board Name String	<nul>	—
20–255	Unused	FFh	FFFFh

## ***GPS6160 Compatibility (Not recommended for new designs)***

GPS6160 Compatibility Register			
ADDR (hex)	REGISTER	DIR	COMMENTS
GPS BASE + 400h	Digital I/O	I/O	Digital I/O Port (GPS6160 compatible only)

### **Digital I/O – R/W at BASE + 400h (GPS6160 compatibility only)**

This register is intended only for GPS6160 compatibility. This address is used to interface to the digital I/O port of the GPS16160. Writing to this address will transfer the data to the output port, while reading from this address will return the data from the digital inputs. This register is compatible with the GPS6160 module. Note the default direction of the 16 digital I/O bits is bits 0 - 7 are outputs and 8 - 15 are inputs. Note: If you change the direction registers from the default, then this register will not operate properly.

Digital I/O – Write GPS BASE + 400h (GPS6160 Compatibility Only)		
Bit 0	Output 0	CN8 Pin 2
Bit 1	Output 1	CN8 Pin 3
Bit 2	Output 2	CN8 Pin 4
Bit 3	Output 3	CN8 Pin 5
Bit 4	Output 4	CN8 Pin 6
Bit 5	Output 5	CN8 Pin 7
Bit 6	Output 6	CN8 Pin 8
Bit 7	Output 7	CN8 Pin 9

Digital I/O – Read GPS BASE + 400h (GPS6160 Compatibility Only)		
Bit 0	Input 0	CN8 Pin 12

<b>Digital I/O – Read</b> <b>GPS BASE + 400h</b> <b>(GPS6160 Compatibility Only)</b>		
Bit 1	Input 1	CN8 Pin 13
Bit 2	Input 2	CN8 Pin 14
Bit 3	Input 3	CN8 Pin 15
Bit 4	Input 4	CN8 Pin 16
Bit 5	Input 5	CN8 Pin 17
Bit 6	Input 6	CN8 Pin 18
Bit 7	Input 7	CN8 Pin 19

## ***GPS Software Interface***

### **Reading the GPS Data**

At power-up, the GPS16160 starts transmitting GPS data. Since the board is UART-based, it appears as a standard COM port to the CPU. The user can open a terminal program (e.g. Windows HyperTerminal) and observe the incoming GPS data.

Any software application that interfaces with the GPS must “open” the COM port of the GPS and read the incoming data. This is typically done via the serial port drivers of the operating system. Consult your operating system’s documentation for information.

### **Selecting the GPS Protocol**

The iTrax03-02 outputs GPS data in two protocols: NMEA-0183 or iTalk. At power-up, the board defaults to NMEA-0183.

NMEA-0183 is an ASCII-based GPS message format. It is a standard format, used by many popular GPS engines. Many commercial third-party GPS programs are written for this protocol.

iTalk is a proprietary binary protocol supported by Fastrax GPS engines. It is primarily used by the Fastrax iSuite SDK.

The control registers are used to select which protocol is used. A user application can select the GPS protocol at runtime by manipulating the appropriate bit.

### **Parsing the GPS Data**

To actually get the longitude, latitude, etc, the application running on the host PC must parse the incoming GPS data. The algorithm for parsing the GPS data will depend on the protocol (NMEA or iTalk).

A complete explanation of GPS protocols and how to parse them is beyond the scope of this manual. See the Additional Information section for the protocol specifications.

RTD provides sample applications which demonstrate how to parse the GPS protocols. Source code is also provided. These samples can be used as a starting point to develop your own GPS application.

## **Fastrax iSuite SDK**

Fastrax provides the iSuite Software Development Kit, which can be used to create GPS applications. See the Additional Information section of this manual for more information. Note that iSuite relies on the iTalk protocol, so you must switch the board into iTalk mode before using iSuite.

## ***Interrupts Programming Information***

### ***What is an interrupt?***

An interrupt is an event that causes the processor in your computer to temporarily halt its current process and execute another routine. Upon completion of the new routine, control is returned to the original routine at the point where its execution was interrupted.

Interrupts are a very flexible way of dealing with asynchronous events. Keyboard activity is a good example; your computer cannot predict when you might press a key and it would be a waste of processor time to do nothing whilst waiting for a keystroke to occur. Thus the interrupt scheme is used and the processor proceeds with other tasks. When a keystroke finally occurs, the keyboard then 'interrupts' the processor so that it can get the keyboard data. It then places it into the memory, and then returns to what it was doing before the interrupt occurred. Other common devices that use interrupts are A/D boards, network boards, other used serial ports etc.

### ***Interrupt request lines***

To allow different peripheral devices to generate interrupts on the same computer, the PC AT bus has interrupt request channels (IRQ's). A rising edge transition on one of these lines will be latched into the interrupt controller. The interrupt controller checks to see if the interrupts are to be acknowledged from that IRQ and, if another interrupt is being processed, it decides if the new request should supersede the one in progress or if it has to wait until the one in progress has been completed. The priority level of the interrupt is determined by the number of the IRQ as follows; IRQ0 has the highest priority whilst IRQ15 has the lowest. Many of the IRQ's are already used by the standard system resources, IRQ0 is dedicated to the internal timer, IRQ1 is dedicated to the keyboard input, IRQ3 for the serial port COM2, and IRQ4 for the serial port COM1. Often interrupts 2,5,7,10,11 and 15 are free for the user.

### ***8259 Programmable Interrupt Controller***

The chip responsible for handling interrupt requests in a PC is the 8259 Interrupt Controller. To use interrupts you will need to know how to read and set the 8259's internal interrupt mask register (IMR) and how to send the end-of-interrupt (EOI) command to acknowledge the 8259 interrupt controller.

### ***Interrupt Mask Register (IMR)***

Each bit in the interrupt mask register (IMR) contains the mask status of the interrupt line. If a bit is set (equal to 1), then the corresponding IRQ is masked, and it will not generate an interrupt. If a bit is cleared (equal to 0), then the corresponding IRQ is not masked, and it can then generate an interrupt. The interrupt mask register is programmed through port 21h.

### ***End-of-Interrupt (EOI) Command***

After an interrupt service routine is complete, the 8259 Interrupt Controller must be acknowledged by writing the value 20h to port 20h.

### ***What exactly happens when an interrupt occurs?***

Understanding the sequence of events when an interrupt is triggered is necessary to correctly write interrupt handlers. When an interrupt request line is driven high by a peripheral device (such as the GPS16160), the interrupt controller checks to see if interrupts are enabled for that IRQ. It then checks to see if other interrupts are active or requested and determines which interrupt has priority. The interrupt controller then interrupts the processor. The current code segment (CS), instruction pointer (IP), and flags are pushed onto the system stack, and a new set of CS and IP are loaded from the lowest 1024 bytes of memory.

This table is referred to as the interrupt vector table and each entry to this table is called an interrupt vector. Once the new CS and IP are loaded from the interrupt vector table, the processor starts to execute code from the new Code Segment (CS) and from the new Instruction Pointer (IP). When the interrupt routine is completed, the old CS and IP are popped from the system stack and the program execution continues from the point where interruption occurred.

### ***Using Interrupts in your Program***

Adding interrupt support to your program is not as difficult as it may seem especially when programming under DOS. The following discussion will cover programming under DOS. Note that even the smallest mistake in your interrupt program may cause the computer to hang up and will only restart after a reboot. This can be frustrating and time-consuming.

### ***Writing an Interrupt Service Routine (ISR)***

The first step in adding interrupts to your software is to write an interrupt service routine (ISR). This is the routine that will be executed automatically each time an interrupt request occurs for the specified IRQ. An ISR is different from other sub-routines or procedures. First on entrance the processor registers must be pushed onto the stack before anything else! Second, just before exiting the routine, you must clear the interrupt on the GPS16160 by writing to the Status register, and write the EOI command to the interrupt controller. Finally, when exiting the interrupt routine the processor registers must be popped from the system stack and you must execute the IRET assembly instruction. This instruction pops the CS, IP and processor flags from the system stack. These were pushed onto the stack when entering the ISR.

Most compilers allow you to identify a function as an interrupt type and will automatically add these instructions to your ISR with one exception: most compilers do not automatically add the EOI command to the function, you must do it yourself. Other than this and a few exceptions discussed below, you can write your ISR as any code routine. It can call other functions and procedures in your program and it can access global data. If you are writing your first ISR, we recommend you stick to the basics; just something that enables you to verify you have entered the ISR and executed it successfully. For example: set a flag in your ISR and in your main program check for the flag.

**Note:** If you choose to write your ISR in in-line Assembly, you must push and pop registers correctly and exit the routine with the IRET instruction instead of the RET instruction.

There are a few precautions you must consider when writing ISR's. The most important is, **do not use any DOS functions or functions that call DOS functions from an interrupt routine.** DOS is not re-entrant; that is, a DOS function cannot call itself. In typical programming, this will not happen because of the way DOS is written. But what about using interrupts? Consider then the following situation in your program: If DOS function X is being executed when an interrupt occurs and the interrupt routine makes a call to the same DOS function X, then function X is essentially being called while active. Such cases will cause the computer to crash. DOS does not support such operations. The general rule is do not call any functions that use the screen, read keyboard input or any file I/O routines, these should not be used in ISR's.

The same problem of reentrancy also exists for many floating-point emulators. This effectively means that you should also avoid floating point mathematical operations in your ISR.

Note that the problem of reentrancy exists, no matter what programming language you use. Even, if you are writing your ISR in Assembly language, DOS and many floating point emulators are not re-entrant. Of course there are ways to avoid this problem, such as those which activate when your ISR is called. Such solutions are, however, beyond the scope of this manual.

The second major concern when writing ISR's is to make them as short as possible in term of execution time. Spending long times in interrupt service routines may mean that other important interrupts are not serviced. Also, if you spend too long in your ISR, it may be called again before you have exited. This will lead to your computer hanging up and will require a reboot.

Your ISR should have the following structure:

Push any processor registers used in your ISR.

Put the body of your routine here

Clear the interrupt bit by reading GPS16160 RXD register  
Issue the EOI command to the 8259 by writing 20h to 20h  
Pop all registers. Most C compilers do this automatically

The following C example shows what the shell of your ISR should be like:

```
/*-----  
| Function:      new_IRQ_handler  
| Inputs:        Nothing  
| Returns:       Nothing  
|-----*/  
void interrupt far new_IRQ_handler(void)  
{  
    IRQ_flag = 1;          // Indicate to process interrupt has occurred  
    {  
        // Your program code to read UART  
        // read to a data buffer for example:  
        Guc_buffer[Gi_bufpos++] = inp(gi_SERIAL_DATA);  
    }  
    outp(0x20, 0x20);      // Acknowledge the interrupt controller  
}
```

### ***Saving the Startup Interrupt Mask Register (IMR) and interrupt vector***

The next step after writing the ISR is to save the startup-state of the interrupt mask register, (IMR) and the original interrupt vector you are using. The IMR is located in address 21h. The interrupt vector you will be using is located in the interrupt vector table which is an array of pointers (addresses) and it is located in the first 1024 bytes of the memory (Segment 0 offset 0). You can read this value directly, but it is better practice to use DOS function 35h (get interrupt vector) to do this. Most C compilers have a special function available for doing this. The vectors for the hardware interrupts on the XT - bus are vectors 8-15, where IRQ0 uses vector 8 and IRQ7 uses vector 15. Thus if your GPS16160 is using IRQ5 it corresponds to vector number 13.

Before you install your ISR, temporarily mask out the IRQ you will be using. This prevents the IRQ from requesting an interrupt while you are installing and initializing your ISR. To mask the IRQ, read the current IMR at I/O port 21h, and set the bit that corresponds to the IRQ. The IMR is arranged so that bit 0 is for IRQ0 and bit 7 is for IRQ7. See the paragraph entitled *Interrupt Mask Register (IMR)* earlier in this discussion for help in determining your IRQ's bit. After setting the bit, write the new value to I/O port 21h.

With the startup IMR saved and the interrupts temporarily disabled, you can assign the interrupt vector to point to your ISR. Again you can overwrite the appropriate entry in the vector table with

a direct memory write, but this is not recommended. Instead use the DOS function 25h (Set Interrupt Vector) or, if your compiler provides it, the library routine for setting up interrupt vectors. Remember that interrupt vector 8 corresponds to IRQ0, vector 9 for IRQ1 etc.

If you need to program the source of your interrupts, do that next. For example, if you are using transmitted or received messages as an interrupt source program it to do that. Finally, clear the mask bit for your IRQ in the IMR. This will enable your IRQ.

### ***Common Interrupt mistakes***

Remember hardware interrupts are from 8-15, XT IRQ's are numbered 0-7. Do not forget to clear the IRQ mask bit in the IMR Forgetting to send the EOI command after ISR code. Disables further interrupts.

### **Example on Interrupt vector table setup in C-code:**

```
void far _interrupt new_IRQ1_handler(void);          /* ISR function */
#define IRQ1_VECTOR 3                               /* Name for IRQ */
void (interrupt far *old_IRQ1_dispatcher)
    (es,ds,di,si,bp,sp,bx,dx,cx,ax,ip,cs,flags);    /* Variable to store old IRQ_Vector */
void far _interrupt new_IRQ1_handler(void);

/*-----
| Function:    init_irq_handlers
| Purpose:     Set the pointers in the interrupt table to point to
|              our functions i.e. setup for ISR's.
|-----*/
void init_irq_handlers(void)
{
    _disable();
    old_IRQ1_handler = _dos_getvect(IRQ1_VECTOR + 8);
    _dos_setvect(IRQ1_VECTOR + 8, new_IRQ1_handler);
    Gi_old_mask = inp(0x21);
    outp(0x21,Gi_old_mask & ~(1 << IRQ1_VECTOR));
    _enable();
}

/*-----
| Function:    restore, do this before exiting program
| Purpose:     Restore the interrupt vector table.
|-----*/
void restore(void)
{
    /* Restore the old vectors */
    _disable();
    _dos_setvect(IRQ1_VECTOR + 8, old_IRQ1_handler);
    outp(0x21,Gi_old_mask);
    _enable();
}
```

# GPS16160 Specifications

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## ***GPS16160 Specifications***

- PC/104 interface
  - 8-bit, 8.25 MHz (typical)
  - Individual ISA Interrupt for GPS and 1 PPS
- UART
  - 16C550 with 16 byte FIFOs
  - Oscillator frequency 1.8432 MHz
- Digital I/O
  - 16 bit-programmable (GPS6160 mode is 8 in and 8 out)
  - Jumper selected 10K pull up/down in 8-bit blocks
- Size: 3.6"L x 3.8"W x 0.6"H (90mm L x 96mm W x 15mm H)
- Weight: 0.24bs (0.10 Kg)
- Power Consumption: 2W @ 5 VDC Typical

## ***Fastrax iTrax03-02 GPS Receiver Specifications***

Specifications (based on 3.31 firmware)

General:

- L1 frequency, C/A code (SPS)
- 12 independent tracking channels
- Separate search and acquisition engine

Update rate:

- 1 fix/s (user configurable up to 3Hz)

Accuracy:

- Position: 1.0 m (CEP50)  
1.2 m (CEP95)
- Velocity: 0.1 m/s
- Time: 20 ns RMS

Time to first fix:

- Out of the box 40 s typical
- Cold Start 36 s typical
- Hot start: 4 s typical

Sensitivity:

- Acquisition (cold): -141 dBm
- Acquisition (hot, warm): -149 dBm
- Tracking: -156 dBm
- Navigation: -155 dBm

Power Drain

- Navigating 1 fix/s: 95mW typical
- Idle Mode: 15mW typical



- Sleep Mode: 60uW typical
- Operating temperature: -40°C to +85°C
- Storage temperature: -40°C to +85°C
- Flash memory:
  - iTrax03-02/8 8MBit
- I/O ports:
  - Two asynchronous serial ports (only one connected to CPU at a time)
  - 1 PPS output
- Protocol:
  - NMEA 0183
  - iTalk Binary Protocol
- Antenna Input:
  - 50 ohm
  - MCX straight jack receptacle connector
- Antenna bias:
  - External input
- Chipset:
  - u-Nav uN8021 RF
  - u-Nav uN8130 Baseband
- SW Features:
  - Kalman Navigation
  - Reprogramming on the fly
  - Advanced Multipath Mitigation
  - Advanced Cross Correlation Mitigation
  - Data-logger
  - A-GPS Support
  - WAAS / EGNOS Support
  - INS support
  - Automatic Interval mode

## ***GPS16160 Operating Conditions***

Cooling	Convection
Operating temperature	-40° to +85° C
Humidity	RH up to 95% non-condensing
Storage temperature range	-40° C to +85° C

## **Additional Information**

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### ***Fastrax iTrax03-0202 GPS Receiver***

For a downloadable datasheet for the iTrax03-02 GPS receiver visit the receiver Fastrax's website:

[www.fastraxgps.com](http://www.fastraxgps.com)

### ***NMEA-0183 v2.01 Standard***

For a complete description on the National Marine Electronics Association (NMEA-0183) protocol visit the Fastrax website:

[www.fastraxgps.com](http://www.fastraxgps.com)

# Limited Warranty

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RTD Embedded Technologies, Inc. warrants the hardware and software products it manufactures and produces to be free from defects in materials and workmanship for one year following the date of shipment from RTD EMBEDDED TECHNOLOGIES, INC. This warranty is limited to the original purchaser of product and is not transferable.

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